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US-PAT-NO: 5923859
DOCUMENT-IDENTIFIER: US 5923859 A

TITLE: Dual arbiters for arbitrating access to a first and second bus in a computer system having bus masters on each bus

DATE-ISSUED: July 13, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Melo; Maria L.	Houston	TX		
Lester; Robert Allan	Houston	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Compaq Computer Corporation	Houston	TX			02

APPL-NO: 08/ 974149 [PALM]
DATE FILED: November 19, 1997

PARENT-CASE:
This is a continuation of application Ser. No. 08/421,202, filed on Apr. 13, 1995 now abandoned.

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/293; 395/294, 395/299, 395/728, 395/726
US-CL-CURRENT: 710/113; 710/114, 710/119, 710/200, 710/240

FIELD-OF-SEARCH: 395/293, 395/294, 395/299, 395/726, 395/728

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4755938	July 1988	Takahashi et al.	
☐	4980854	December 1990	Donaldson et al.	
☐	4987529	January 1991	Craft et al.	364/200
☐	5067071	November 1991	Schanin et al.	

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☐	5083260	January 1992	Tsuchiya	395/325
☐	5151994	September 1992	Wille et al.	
☐	5191656	March 1993	Forde, III et al.	
☐	5212796	May 1993	Allison	395/725
☐	5301282	April 1994	Amini et al.	395/325
☐	5317696	May 1994	Hilgendorf	
☐	5333274	July 1994	Amini et al.	395/275
☐	5392436	February 1995	Jansen et al.	395/725
☐	5438666	August 1995	Craft et al.	395/842
☐	5448742	September 1995	Bhattacharya	395/481
☐	5524235	June 1996	Larson et al.	395/478
☐	5528766	June 1996	Ziegler et al.	395/293
☐	5535395	July 1996	Tipley et al.	395/729
☐	5596729	January 1997	Lester et al.	395/308

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0374521A2	June 1990	EP	

OTHER PUBLICATIONS

82375EB PCI-EISA Bridge (PCEB) Order Number: 290477-001, Apr. 1993.
82420/82430 PCI SET, ISA and EISA Bridges, Intel Corp., pp. 3-5, 17, 35, 37, 148, 154-157, 172-174, 211, 225-226, 293-302, 320-321, 345, 363-364, 438-444, 460-462 (1993).
Peripheral Components, Intel Corp., pp. 1-215, 1-222 to 1-225, 1-245 to 1-246, 1-265 to 1-267, 1-280 to 1-285 (1993).

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Thlang; Eric S.

ATTY-AGENT-FIRM: Akin, Gump, Strauss, Hauer & Feld, L.L.P.

ABSTRACT:

Arbitration circuitry in a computer system having a plurality of arbiters for arbitrating requests from bus masters on a PCI bus and an EISA bus. Each of the PCI and EISA buses have a plurality of masters. The PCI bus utilizes a modified LRU arbitration scheme, while the EISA bus utilizes a rotating priority scheme. The arbiter on the EISA bus includes a first level of arbitration and a second level of arbitration. The first level is assigned a plurality of requester types to determine the priority between the requestor types. Certain of the first level requestor types include a plurality of devices. If one of those certain requestor types wins priority on the first level arbitration cycle, a second level

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arbitration is performed to determine the priority between the plurality of devices.

32 Claims, 20 Drawing figures

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